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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,994	07/24/2003	Curtis B. Robinson JR.	386168016US	4169

25096 7590 04/04/2005

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EXAMINER

LAXTON, GARY L

ART UNIT	PAPER NUMBER
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2838

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

<b>Office Action Summary</b>	<b>Application No.</b> 10/626,994	<b>Applicant(s)</b> ROBINSON, CURTIS B.	
	<b>Examiner</b> Gary L. Laxton	<b>Art Unit</b> 2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 January 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 1/26/05 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the APA figure 1 with the Hugel reference, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Hugel et al disclose that a problem with conventional amplifiers is they incur DC offset and temperature drift problems, and accordingly the present invention of Hugel et al suggests motivation by expressly teaching that in order to overcome the DC offset and temperature drift problem of conventional amplifiers, the invention provides a current feedback to the input of a transimpedance amplifier.

Additionally, applicant argues that Hugel neither attempts to solve the problem being solved by the present invention nor does it even address the problem. The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the

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differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Applicant further continues by arguing that Hugel does not compare two currents for regulating the output voltage. The examiner respectfully draws the applicant's attention to figure 4 of the drawings and to col. 6 lines 42-49 of the specification wherein Hugel expressly states "The other side of the resistor 66 is coupled to a common node 68 in the comparing means 20 that receives a current signal from the current sensing means 22. The variable resistor 66 is adjusted empirically so that the same amount of current is flowing through resistor 66 and into node 68 as is flowing from FET 74 into node 68 (FET 74 acts as a voltage-to-current converter). Therefore, there is no merit to applicant's argument concerning Hugel and therefore, the examiner respectfully maintains the rejection of the claims accordingly.

### ***Claim Objections***

2. Claims 1-11 are objected to because of the following informalities: applicant uses the limitation "voltage representative current"; it is unclear whether this is a voltage that is representing or is proportional to a current; or whether this is a current represented as or by a voltage or if this is a voltage represented as a current or whether this is a current that is representing or is proportional to a voltage. Clarification would be appreciated. Applicant's remarks seem to add confusion. See applicants remarks page 6 lines 6-8: "...Hugel does not compare two currents for regulating the output voltage, while such comparison is an important feature of the present invention."; and

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see page 8 line 21: "In contrast, the received signal in the present invention is a voltage signal". See also specification page 4 paragraph [0015] lines 7-9 of the paragraph: the current in the sense pin is an analog representation of the voltage. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 and 3-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art figure 1 (APA fig 1) in view of Hugel et al (US 5,886,581).

Claims 1 and 3-8; APA fig 1 discloses a method of controlling the output voltage of a voltage regulator by measuring an output voltage and comparing the output voltage to a reference voltage in order to calculate the voltage error difference and to stop a charging process by controlling a power switch in response to the error voltage when the error signal is the same as the reference voltage. The regulator also uses a transformer to provide the output voltage.

However, APA fig 1 does not disclose measuring a voltage representative current of the output; comparing the voltage representative current to a reference current; and stopping a charging process of the voltage regulator when the voltage representative current of the output is substantially the same as the reference current.

Hugel et al teach a voltage regulator (30) using a transimpedance amplifier (24) for calculating a current error signal based on a current measurement (22) to control the voltage regulator based on the current error signal. Furthermore, Hugel et al teach that conventional amplifiers incur DC offset and temperature drifts problems and Hugel et al teach providing current feedback to the input of a transimpedance amplifier to overcome these problems (col. 1 lines 34-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the regulator circuit of the APA fig 1 to include a transimpedance amplifier in the regulator circuit and to measure a voltage representative current of the output; comparing the voltage representative current to a reference current; and stopping a charging process of the voltage regulator when the voltage representative current of the output is substantially the same as the reference current.

Claims 9-11; APA fig 1 discloses a voltage regulator operative to monitor an output voltage on an output, the voltage regulator comprising: voltage comparator having a reference input and a sense input, the sense input connected to the output through a resistor or resistor divider, the comparator indicating that the output voltage is nominal when the sense input and the reference input are in a predetermined relation.

However, APA fig 1 does not disclose the comparator being a transimpedance block.

Hugel et al teach a voltage regulator (30) using a transimpedance amplifier (24) for calculating a current error signal based on a current measurement (22) to control the voltage regulator based on the current error signal. Furthermore, Hugel et al teach that conventional amplifiers incur DC offset and temperature drifts problems and Hugel et al teach providing

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current feedback to the input of a transimpedance amplifier to overcome these problems (col. 1 lines 34-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the regulator circuit of the APA fig 1 to include a transimpedance block in the regulator circuit in place of the voltage comparator in order to overcome the DC offset and temperature drifts normally associated with voltage comparators as taught by Hugel et al.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art figure 1 (APA fig 1) and Hugel et al (US 5,886,581) in view of Wilcox et al (US 5,731,694).

Claim 2; APA fig 1 and Hugel et al disclose the claimed subject matter in regards to claim 1 except for the reference current is generated by the use of a voltage reference and a voltage to current converter.

Wilcox et al teach converting a voltage to a current by converting a voltage reference (37) into a current through a voltage to current converter (38, 38A) in order to compare a measured current ( $I_{FB}$ ) to a current reference (38A) which is derived from a reference voltage (37).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify APA fig 1 and Hugel et al to include a reference current that is generated by the use of a voltage reference and a voltage to current converter as taught by

Wilcox et al in order to compare a measured current to a current reference which is derived from a reference voltage.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,856,519 Lin et al teaches a controller and feedback loop capable of controlling a DC/DC converter output voltage by using an error amplifier (30) that operates as a current source (e.g., transconductance amplifier) to adjust the charge on a capacitor (40). Transconductance amplifier (30) compares the load current  $I_{sens}$  to a user-definable reference signal (32) indicative of maximum load current. If the value of the load current is less than signal (32), transconductance amplifier 30 will source current to charge the capacitor (40) in an attempt to increase the DC value of an error signal (52), to thereby increase the pulse width of the output driver signals. If the value of the load current is greater than the reference signal (32), transconductance amplifier (30) will cease charging capacitor (40) and proceed to sink charge from capacitor (40) to decrease the DC value of the error signal (52), thereby decreasing the pulse width of the output driver signals. In other words, transconductance amplifier (30) represents a closed loop feedback current control that sources (charging current) or ceases charging and sinks current to maintain the load current  $I_{sens}$  approximately equal to the reference signal (32). According, Lin et al teach a transimpedance block as an amplifier comprising: measuring a current of an output; comparing the current to a reference



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current and stopping a charging process of the converter when the current of the output is substantially the same as reference current.


7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Gary L. Laxton  
Primary Examiner  
Art Unit 2838  
3/31/05